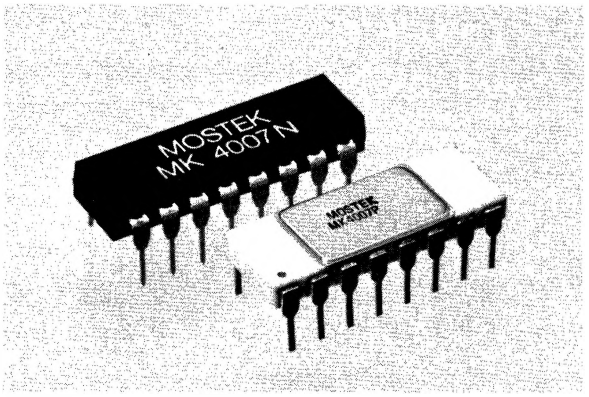
MK 4007P
MK 4007N

256 BIT
MOS Random Access Memory

MOSTEK



FEATURES:

- ☐ Versatile RAM can replace any existing 1101-type 256x1 MOS RAM pin for pin.
- ☐ Ion-implanted for superior performance.
- ☐ **Lower power dissipation:** TOTAL 370 mW max over entire temperature range.
- ☐ **Faster access time:** Typically 525 ns with V_D and V_{DD} at −9V.
- ☐ **Less temperature-sensitive:** specified over entire AMBIENT temperature range 0° to 75°C.
- ☐ **Tight control of output sink current capabilities:** made possible by use of depletion-mode transistors.
- ☐ **No restrictions** on address input sequence, skew, or rise and fall times.
- ☐ Full DTL/TTL compatibility.
- ☐ Wide power supply range: +5V; −6.5 to −15V.

APPLICATIONS:

Ideal for small buffer storage requiring low cost, superior performance, and bipolar compatibility, such as:

- ☐ Scratchpad memories
- ☐ Data link buffers
- ☐ Key-to-tape buffers
- ☐ Tape-to-printer buffers
- ☐ Editing memories.

DESCRIPTION

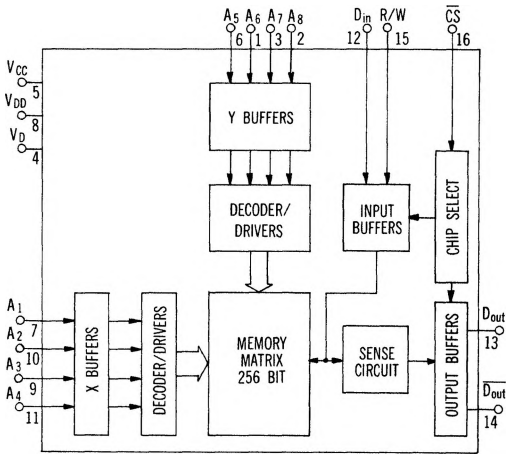
Ion-implantation processes used in manufacturing the Mostek MK 4007 P Random Access MOS Memory result in a low-cost device with performance exceeding other industry types over the entire temperature and voltage supply ranges. It may be used to replace any existing 1101 type RAM pin for pin.

The depletion-load ion-implantation technique allows the fabrication of both depletion and enhancement mode transistors on the same chip. The result is not only superior operating characteristics within the region usually specified for devices of this type, but also wider operational areas without severe performance degradation. For example, while specifications for this device are given for V_D and V_{DD} from −7 to −13.2V, V_D and V_{DD} may actually range from −6.5 to −15 V (see DC Operating Conditions and Fig. 1). Access times are improved (see Fig. 2); power dissipation is reduced (see Fig. 3) and output sink current capabilities are improved (see Fig. 4). The device is less temperature-dependent (see Figures 5 and 6) and is specified over the *entire* ambient temperature range of 0° to 75°C.

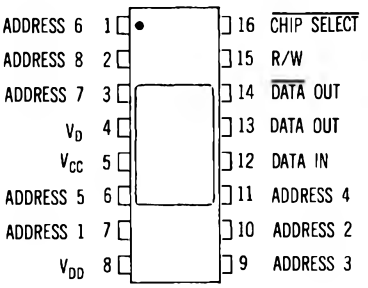
The ion-implantation process also makes the MK 4007 P RAM fully TTL/DTL compatible at all inputs and outputs.

The 4007 P is a static memory, requiring no clocks or refreshing. Data is written into the address location by applying a logic "1" to the R/W input. Addressing the desired location, with the chip enabled and R/W at logic "0", provides a non-destructive read-out (NDRO) of true and complement data. A "Chip Select" allows output buffers to be open-circuited during disable time for wire ORing. All inputs are protected against static charge accumulation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{CC} . . . . . + 0.3 V to −25 V
Operating Temperature Range (Ambient) . . . . . .0°C to +75°C
Storage Temperature Range (Ambient) . . . . . .−55° to +150°C

DC OPERATING CONDITIONS

(Ambient Temperature Range: 0°C to +75°C)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
	V_{DD}	Supply Voltage	−6.5	−9.0	−15.0	V	See Fig. 1 for
	V_D	Supply Voltage	−6.5	−9.0	−15.0	V	V_D, V_{DD} differential
INPUTS	V_{IL}	Logic "0" Voltage, any input		0	+0.8	V	
	V_{IH}	Logic "1" Voltage, any input	V_{CC} −2.0	V_{CC}	V_{CC}+0.3	V	

ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%;
$V_D = V_{DD}$ = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP(1)	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current. V_D		8.0	16	mA	$V_D = V_{DD}$ = −9V ± 5%
	I_{DD}	Supply Current, V_{DD}		4.0	9	mA	Outputs open-circuited.
	P_D	Power Dissipation, Total		170	370	mW	
	I_D	Supply Current. V_D			19	mA	$V_D = V_{DD}$ = −13.2 V
	I_{DD}	Supply Current, V_{DD}			10	mA	V_{CC} = +5.25 V
	P_D	Power Dissipation, Total			535	mW	Outputs open-circuited.
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	$V_D = V_{CC}$; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = 0 V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. meas. =
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	1 MHz; Tested input = V_{CC}
OUTPUTS	I_{OL}	Output Current, Logic "0"	3.2	5.6		mA	V_O = +0.40 V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	$V_O = V_{CC}$ −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; $V_O = V_{CC}$

NOTES:

(1) Typical values at V_{CC} = +5 V, $V_D = V_{DD}$ = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

TIMING

(Ambient Temperature Range: 0°C to 75°C; V_{CC} = +5 V ±5%; $V_D = V_{DD}$ = −7V to −13.2 V, unless otherwise specified. See Notes 1 and 2.)

		PARAMETER	MIN	TYP	MAX	UNITS	
OPERATING CONDITIONS	t_{wc}	Write Cycle Time	700			ns	
	t_{wd}	Write Set-up Delay	300			ns	
	t_{wp}	Write Pulse Width	400			ns	
	t_{dld}	Data Lead Time	300			ns	
	t_{dlg}	Data Lag Time	0			ns	
	t_{cw}	Chip Select Pulse Width	400			ns	
DYNAMIC CHAR.	t_{ACC}	Access Time		525	900	ns	$V_D = V_{DD}$ = −9V ±5%.
	t_{RC}	Read Cycle Time			800	ns	(See Note 3.)
	t_{ACC}	Access Time			1.0	µs	$V_D = V_{DD}$ = −7V to −13.2V.
	t_{RC}	Read Cycle Time			900	ns	(See Note 3.)
	t_{OH}	Data Output Hold Time	100			ns	
	t_{CSE}	Chip-Select-to-Output Enable			300	ns	
	t_{CSD}	Chip-Select-to-Output Disable			300	ns	

Random Access Memories

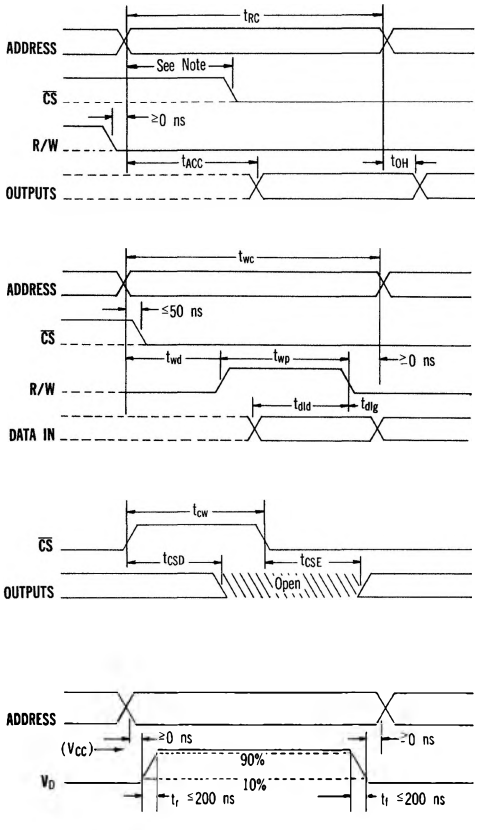
NOTES:

(1) All measurements to the 1.5 V level; inputs for test are 0 to 5 V and ≤10 ns rise and fall times; output is loaded with 1 TTL and approx. 20 pF.

(2) R/W should be brought to logical "0" whenever address bits are changed; however, there are no restrictions on rise and fall times of address bits, nor on the sequence (or skew) of address bit changes.

(3) Read Cycle may be "pipe-lined," i.e., the minimum hold time (t_{OH}) may be subtracted from the maximum access time (t_{ACC}).

TIMING



READ CYCLE

Reading is accomplished with R/W (Read/Write) and $\overline{CS}$ (Chip Select) at logical "0."

NOTE: $\overline{CS}$ logical "1" overlap time shown must be 300 ns (max t_{CSE}) less than the desired access time; e.g., if desired access time t_{ACC} = 1.2 µs, then $\overline{CS}$ should go to logical "0" no later than 900 ns following address change.

WRITE CYCLE

Writing is accomplished with R/W at logical "1" and $\overline{CS}$ at logical "0." $\overline{CS}$ at logical "1" may overlap the address change as much as 50 ns. R/W may be taken to logical "0" coincidentally with an address change, but should not overlap an address change while in the logical "1" state.

CHIP SELECT

$\overline{\text{Chip Select}}$ at logical "1" causes the normal push-pull output buffers to be open-circuited for purposes of wire-ORing. The $\overline{\text{Chip Select}}$ may be used to access the memory at a faster rate by maintaining a constant address and selecting individual chips with the $\overline{\text{Chip Select}}$ input.

POWER SWITCHING

During standby operation the MK 4007 P will dissipate only 30 mW of power (typically) if the peripheral power supply, V_D, is reduced to V_{CC}. The R/W input may be maintained at logical "0" or "1"; however, if R/W is at logical "1," $\overline{\text{Chip Select}}$ should also be logical "1" (to disable chip during standby operation). With the return of power, either read or write cycles may commence as described above.

TYPICAL PERFORMANCE CURVES

FIG. 1: POWER SUPPLY OPERATING REGION & DIFFERENTIAL

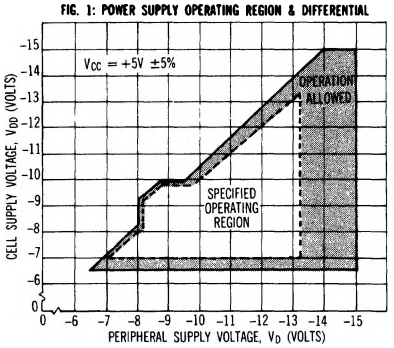


FIG. 2: ACCESS TIME VS SUPPLY VOLTAGE, (V_D)

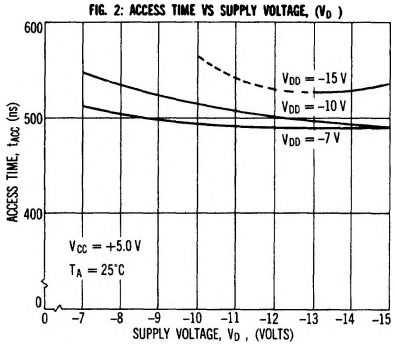


FIG. 3: TOTAL POWER DISSIPATION, (P_D), VS SUPPLY VOLTAGE, (V_D and V_{DD})

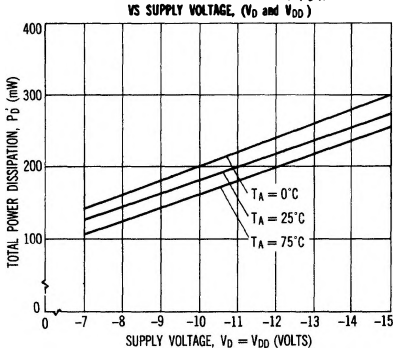


FIG. 4: OUTPUT CURRENT VS OUTPUT VOLTAGE

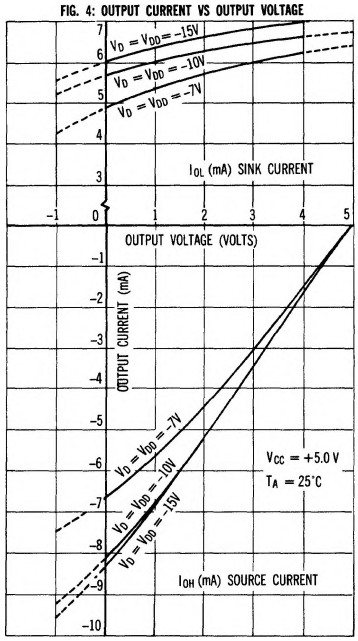


FIG. 5: OUTPUT CURRENT VS AMBIENT TEMPERATURE

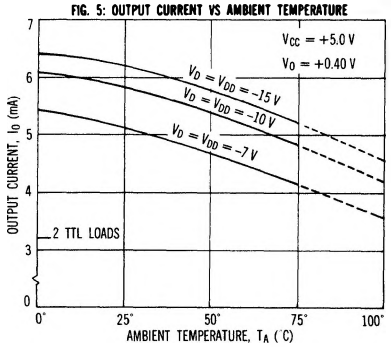


FIG. 6: WORST-CASE ACCESS TIME VS SUPPLY VOLTAGE (At Various Capacitances and Ambient Temperatures)

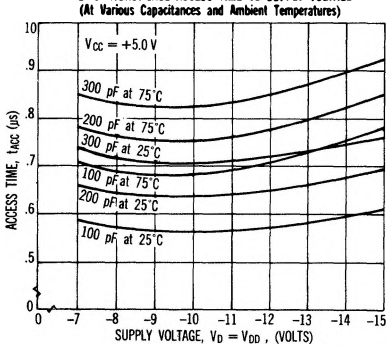


FIG. 7: SUPPLY CURRENT, (I_D and I_{DD}), VS SUPPLY VOLTAGE (V_D and V_{DD})

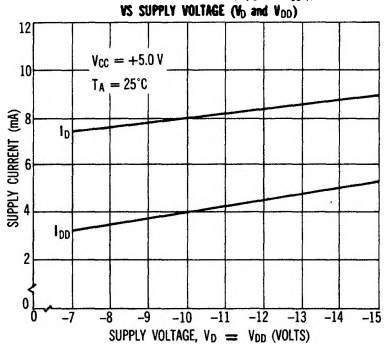
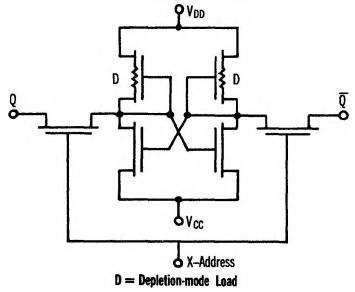
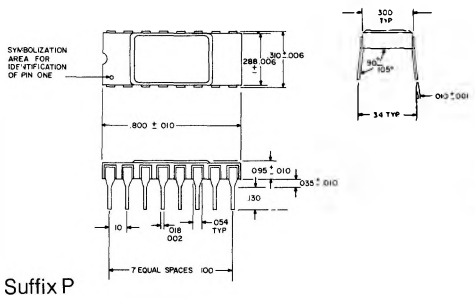


FIG. 8: MK 4007 P MEMORY CELL



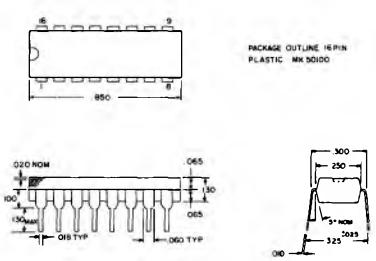
D = Depletion-mode Load

PACKAGE
16-pin ceramic dual-in-line



Suffix P

PACKAGE
16-pin plastic dual-in-line



Suffix N