MR9735

TELETEXT/VIEWDATA 625-LINE VIDEO GENERATOR

The MR9735 Video Generator chip reads the contents of a Page Store and generates outputs suitable for driving a normal 625-line colour television receiver to display the contents of the page store.

The chip also monitors the composite synchronising signals within the receiver and locks onto the incoming interlaced signals. When no transmission is taking place, the chip generates an interlaced or non-interlaced composite sync. signal which is used to synchronise the receiver.

A full set of colour display facilities as described in the Broadcast Teletext Specification (September 1976) is provided by the device.

The MR9735 is fabricated on the GPS N-channel metal gate process, providing direct TTL interfacing, high speed and good reliability.

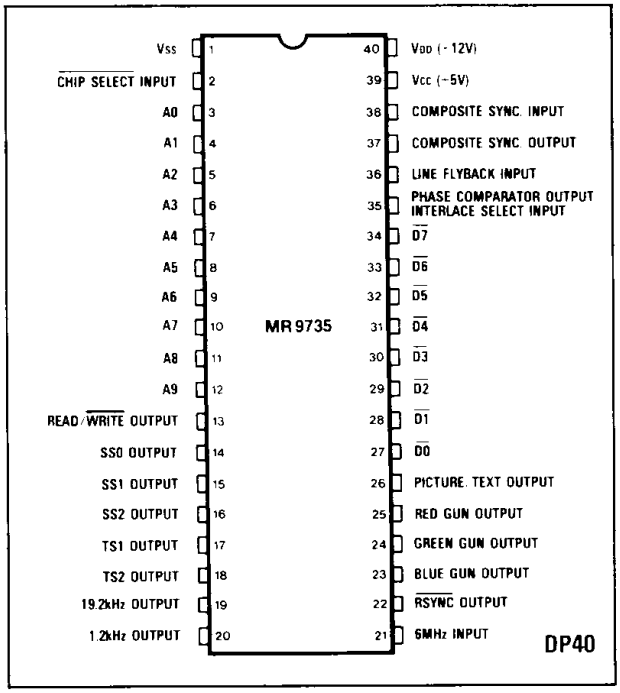


Fig.1 Pin connections - top view

FEATURES

- Interlaced 625 line or non-interlaced 313 line operation
- 24 Row x 40 Character display
- Character Set options available
- On and Off Hours operation
- Half Page Expansion
- Boxed Clock and Header on Teletext
- Can address up to eight Page Stores
- Provides the address information to scan the allocated Page Store
- Provides composite synchronising signals for the receiver for 'Off-Hours' working
- Provides comprehensive set of display facilities

DISPLAY FACILITIES

1. Provides the following display facilities controlled by 'control' characters read from the store i.e. via the TELETEXT/VIEWDATA transmission.

(a) Alpha-numerics/Graphics in seven colour set.

(b) Colour or black backgrounds.

(c) Selected characters can be concealed.

(d) Selected characters can be flashed.

(e) 'Boxed' characters can be inserted into the normal Television Picture. This can be done manually or automatically.

(f) Characters may be either single or double height.

(g) Graphics characters may be contiguous or separated.

(h) Graphics characters may be 'held' during other control characters.

(i) Special graphics for high resolution applications, a dynamically redefinable character set application also available.

2. Provides the following display facilities.

(a) Switch between normal and data video.

(b) Teletext or Viewdata Operation.

(c) Clock time can be boxed into a normal picture (Teletext only).

(d) Display of one half of a page in double height.

(e) Black and white output of data in Mix Mode.

(f) Inhibiting of character rounding and flashing.

(g) Enabling of a cursor.

(h) Inhibit the display until updated.

(i) Reveal 'concealed' characters.

CHARACTER SETS

English	MR9735-002
German	MR9735-003
Swedish/Finnish	MR9735-004
Danish	MR9735-005
Italian	MR9735-006
Others	Contact Factory

PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	This is the negative supply for the chip and is used as a reference for all the electrical parameters.
2	$\overline{\text{Chip Select}}$ Input	The chip can be put in its deselected state by connecting this input to Vcc. The input has an internal pull down to Vss. If connected to Vdd the test mode is selected.
3-12	A0-A9	**These pins are connected to the system Address Bus. They are used for address Input/Output.**
13	Read/$\overline{\text{Write}}$ Output	This output is used to drive the Random Access Memories forming the Page Memory.
14-16	SS0-SS2 Outputs	These binary coded outputs are used to select the required Page Store.
17,18	TS1,TS2 Outputs	These outputs are generated by the Video Generator from the status of the raster scan and are used to indicate this status to other chips within the system.
19,20	19.2kHz and 1.2kHz Outputs	These outputs provide 19.2kHz and 1.2kHz square wave signals which are used by the UAR/T as reception and transmission clocks respectively.
21	6MHz Input	This input is fed from a 6MHz oscillator which is phase locked to the normal transmission for Teletext ON Hours operation. During OFF Hours working a free running crystal oscillator is normally used.
22	$\overline{\text{RSYNC}}$ Output	**This output is an open-drain output and is used to indicate the presence of Teletext lines to the Data Slicer SL9100. The timing of this signal is indicated in Fig. 9.**
23-25	Red, Green and Blue Outputs	These outputs are push-pull outputs which go high to turn on the relevant colour gun for displaying. These outputs are closely matched for propagation delay and rise and fall times.
26	Picture/$\overline{\text{Text}}$ Output	This output may be used by the TV receiver to determine whether to display the normal TV Picture or the generated Text as provided at the Red, Green and Blue outputs. In the mix mode this generates monochrome video. It will then be matched to the gun outputs for propagation delay and rise and fall times.
27-34	$\overline{\text{D0}}$-$\overline{\text{D7}}$ Inputs	The Data Inputs form the communication highway between the Video Generator and the Control Processor and Page Memory.
35	Phase Comparator Output/Interlace Select Input	In on-hours operation the display Line Flyback signal is compared for phase with an internal 64μs period signal derived from the 6MHz display clock. The output is a pulse which produces a voltage for controlling the frequency of a 6MHz display oscillator, thus locking the display to the incoming picture. In off-hours operation this open drain output goes high permanently, and thus can be used as an indication of on-hours/off-hours status. When this output is high the oscillator must run fast and when this output is low the oscillator must run slow. In OFF Hours operation if the Phase Comparator output is held low a 313 line non-interlaced sync. is provided at the Composite Sync. output. If the Phase Comparator output is pulled high connected to Vcc via a 4.7k resistor interlaced sync. will be provided.
36	Line Flyback Input	The Line Flyback input is a signal from the display deflection circuitry which is used for positioning the display on the T.V. screen. Line Flyback pulses are positive. If no Line Flyback is provided in OFF hours mode the display will be positioned so that the start of video is approximately 16μs after the negative edge of line sync.
37	Comp. Sync. Output	This output is an open drain output. In on-hours working or in Picture mode it outputs a regenerated composite sync. signal from the comp. sync. input. In off-hours working it outputs an internally generated composite sync.
38	Comp. Sync. Input	The Composite sync. input monitors the composite sync/video being received and extracts synchronising information and 'on-hours' 'off-hours' information for the Video Generator. This input must be predominantly high for 'off-hours' switching. Sync. pulses are negative.
39	Vcc	This pin is connected to the +5.0V supply.
40	Vdd	This pin is connected to the +10.0V supply.

CHIP DESCRIPTION

The Video Generator Chip contains the logic and control functions to interrogate a selected Page Store and display the contained information at the correct period within the raster scan on a normal TV receiver. The chip also generates the master timing signals TS1 and TS2 which indicate the raster status to the Control processor.
The basic block diagram of the chip is shown in Fig. 4 and major functional blocks are described below.

1. Comp Sync Generator and On Hours Detector

The prime function of this block is to detect negative going sync. signals from the incoming mixed sync. and to synchronise the system with the transmitted signal. When the incoming transmission is turned off, (i.e. goes 'Off-hours'), this is recognised by the detector after at least 300ms of missing sync. pulses. An internally generated Composite Sync signal is then switched to the Composite Sync Out pin. Thus the receiver will continue in lock but synchronised to the Video Generator. Similarly if the normal transmission resumes, the fact that external sync pulses are being received is recognised by the Video Generator and the chip will re-synchronise itself with the incoming transmission. Because the Video Generator is aware of the status of the mixed sync. at all times the chip can detect frame sync., line sync. and even or odd frames. Thus with this information the chip can continuously monitor the current line number. The relevant sections of the line scan are decoded and are indicated externally by the TS1, TS2 time slot outputs. These signals are fully described in Figs.7 and 8, but there are four periods i.e.

(i) Writing to RAM. TS10
This occurs during lines 7 to 22 under external control.

(ii) Reading from RAM. TS00
This occurs under control of the Video Generator chip between lines 48 and 288, and is when the display is active.

(iii) Data Interchange Period. TS11
The interchange of information between Control Processor and Video Generator occurs during this period (lines 23-47).

(iv) Spare TS01
During lines 289–296 the Video Generator does not use the Data Bus.

As the chip is aware of the raster status the chip also starts and stops the address counter/latch combination which is used to scan the relevant Page Memory. The form of the generated sync. pulses are shown in Fig. 5.

2. Character Counter and Address Logic

The address counter is a binary counter which is incremented at the Character Display Rate (1MHz). It can also be loaded from a latch which contains the start address of each character row. Since each character consists of 10 vertical lines of raster scan, the counter is incremented 40 times from a start address and then is reloaded with the same start address ready for the next raster scan of the same forty characters. This occurs nine times. On the last line the counter is incremented an extra once and this new address is stored in the latch. This address being the start address of the next row of forty characters. The above sequence is then repeated.

If displaying only one half of a page with all characters in double height, the Video Generator scans the same forty addresses nineteen times and stores the new address on the twentieth raster scan. If it is in the bottom half of the page, the address counter is initialized to 480.

The display format of 40 characters, each 1μs wide, occurs on a line of 64μs duration thus leaving a border of 12μs at each end of the character row. This address counter is actually started some 4μs before the start of the proper character display thus allowing time for address generation, RAM access time, ROM access time and display processing, these actions being pipelined. Facilities are also provided such that the output address can be reduced by 40 thus allowing accessing of the character in the row above. This is a necessary operation for a 'Double Height' display option which will be described later. This facility is inhibited while displaying one half of a page. The address so produced is presented on the address bus and the required Page Memory is activated by the Store Select Outputs. The address drivers are tristate thus allowing easy bus interface, being active for 40μs starting 3.5–6μs after LFB.

3. Input Latches and Character Read-Only Memory

The data being read from the required Page Memory is placed on the Data Bus and is latched into the Data Bus latches. A total of 450ns is allowed for the RAM read cycle and thus quite slow Random Access memories may be used. Having been latched by the Video Generator chip the seven bit character is used to address the character Read Only Memory. This memory is organised as 96 characters each of 45 dots (5 x 9 array).

4. Data Control Latches (Colour Background Control)

Certain characters indicate to the video generator a change in display status. These characters are contained within columns 0 to 1 of the character set as shown in fig. 7 and may be used to change character colour, background colour, height, etc. These facilities, and the control of them, are fully described in the British Broadcasting Teletext Specification (Sept. 1976) published by the BBC, IBA and BREMA.

5. Output Logic and Drivers

The output logic reads the character ROM into a six bit parallel to serial shift register. This operation occurs at the left-hand side of the character to be displayed, the data in the register is then shifted out at 6MHz (character dot-rate) the data bits selecting between character and background information. This information is used to drive the fast Gun output drivers. These outputs are closely matched for propagation delay and rise and fall time to ensure good legibility.

DATA INTERCHANGE

During the TS11 timeslot the Video Generator can receive information from other devices attached to the system buses. This is normally used by the control chip to update the control and display latches within the Video Generator. The Video Generator is enabled to receive by putting the address 1111XX0XXX on the address highway (active high).

The latches are updated by the following control words, active low signalling, most significant bit is a strobe.

Highway Free	0	0	0	0	0	0	0	0
Control Word 1	1	0	0	0	T	S	s	s
Teletext								
Control Word 2	1	0	0	1	X	C_4	C_6	C_5
Control Word 3	1	0	1	0	C_{10}	C_9	C_8	C_7
Control Word 4	1	0	1	1	C_{14}	C_{13}	C_{12}	C_{11}
Viewdata								
Control Word 2	1	0	0	1	X	F	0	0
Control Word 3	1	0	1	0	b_7	0	b_6	b_5
Control Word 4	1	0	1	1	b_4	b_3	b_2	b_1
Store Select for Display	1	1	0	0	SP	D	d	d
Key Data	1	1	0	1	*	P	*	*
Other Facilities	1	1	1	0	X	BH	M	BC

The Control bits are as follows:-

T	TELETEXT MODE i.e. NOT VIEWDATA
Sss	Identification of Store being written to
Ddd	Identification of Store being displayed from

(a) Teletext

C_4	Erases rows 1-23 of Store defined by Sss and resets Reveal if Sss = Ddd
C_5	Newsflash
C_6	Subtitle
C_7	Suppress Header
C_8	Update Indicator
C_9	No action
C_{10}	Inhibit display
C_{11}	No action
C_{12}-C_{14}	No action (may be programmed to enable and disable the chip)

(b) Viewdata

b_7-b_1	Cursor Control Bits
001 0001	Cursor ON } The two Control Words that make up these codes must be transmitted in numerical order in the same TS11 timeslot
001 0100	Cursor OFF }
F	Form feed or first appearance, Erases store defined by Sss, resets Reveal if Sss = Ddd
SP	Sets Picture/Text to picture (for initialization)
P	P Key presed. Resets Reveal, Half Page Expansion, Newsflash/Subtitle (Auto Box), Suppress header, Inhibit display, Update.
M	Mix Mode
BC	Box Clock (Teletext only)
BH	Box Header (Teletext only)
	For M, BC and BH, the latches are set and reset by the appropriate bit
* * *	These are coded as follows:-
001	Picture/Text Key pressed
010	Reveal/Conceal Key pressed
011	½ Page Key pressed (Cycles Full, Top, Bottom, Full etc).
100	Update/Clear Key pressed
	For 001, 010, 011 and 100, the latches are toggled by the appropriate code
101	Rounding and Flashing OFF (Reset by P Key or new viewdata page)
111	Hold (not used by MR9735)

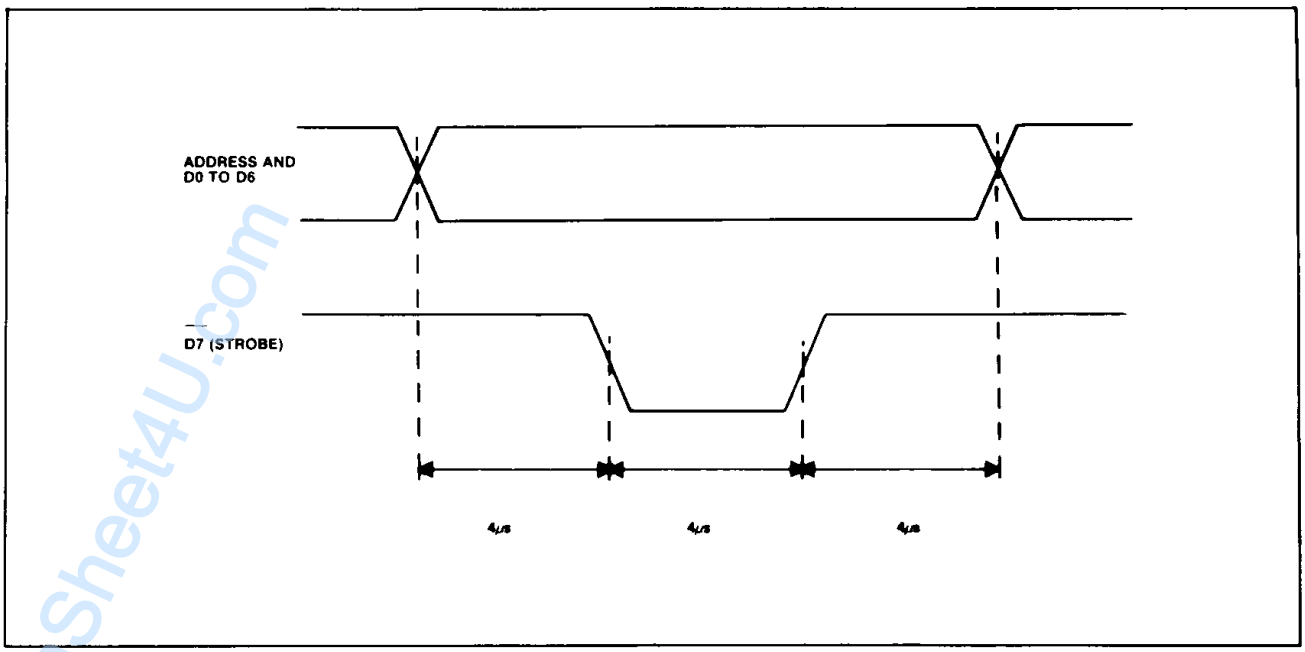


Fig. 2 Typical timing diagram for input data strobing of control data using TS11

DISPLAY OPTIONS

Logic is contained on the Video Generator chip to process the Display Modes as described in the Broadcast Teletext Specification. These facilities are outlined below. Some extra facilities are also included.

1. **Character Set**

The chip can display 96 Alphanumerics characters and 64 Graphics shapes which may be either contiguous or separated. The alphanumeric format is determined by a 4320 bit Read Only Memory organised as:

96 (characters) x 5 (dots) x 9 (lines) = 4320

This can be programmed for different character fonts.

The graphics shapes are determined directly from the bits of the character code (Fig.10).

2. **Display and Background Colour**

The characters and the background can be displayed in one of seven colours. In addition the background may be black. This information is stored in two sets of three latches representing character and background colours.

3. **Conceal and Flash**

Selected characters can be concealed and optionally revealed by the viewer. Selected characters can be flashed on command. The flashing is controlled by an on-chip flash oscillator. During the flash period or when concealed, only background information is displayed. The flash rate is 1.56Hz.

4. **Boxing**

Text or graphics characters can be boxed into a normal video picture. While in Picture mode boxing is automatic if Newsflash or Sub-title (and Sss = Ddd). Other boxed characters may be manually revealed by Reveal command.

5. **Double Height**

Double height characters are characters contained between the control characters "Double Height" and "Normal Height" (or end of line). When a "Double Height" control character is read from the RAM only the top half of the subsequent character(s) are displayed during the 10 raster scans. During the next 10 scan lines, 40 is subtracted from the addresses being output on A0–A9 so the same 40 addresses are read from another 10 times. Characters which are not double height are displayed as the background colour and the bottom(s) of the double height character(s) is (are) displayed.

6. **Hold Graphics**

When this latch is set, any subsequent control characters (except change Double/Normal Height or Change Alpha/Graphics) are displayed as the last graphics character.

7. **Special Graphics**

While in Graphics Mode the Special Graphics command will give a special high resolution facility. In this mode there is a one to one correspondence between data bits b_1, b_2, b_3, b_4, b_5, b_7 and the six dots in each horizontal line of a character. This gives a possible graphics resolution of 6 x 20 for each character in interlace mode (or 6 x 10 if not interlaced).

8. **Box Clock**

When box clock is selected in picture mode and teletext the last eight characters of the page header are boxed in double height. To ensure that the "live" clock is displayed the store address is temporarily switched to that defined by Sss. This function is cleared in text mode.

9. **Box Header**

When box header is selected in picture mode and teletext the page header is boxed in double height (not if bottom half of page selected).

10. **Half-page Operation**

This allows either the top or bottom half of a normal Teletext/Viewdata page to be displayed over the whole screen, with each character in double height. This makes the display easier to read from a distance. Double height characters are ignored in this mode.

11. **Monochrome Output/Mix Mode**

In normal operation the Picture/$\overline{\text{Text}}$ Output is used to blank the normal picture information for boxing or displaying a page of text.

In the mix mode this outputs Monochrome text information which is matched to the Gun Output signals in delay and drive. This can be used to superimpose text onto a picture by "cutting away" the picture below text data or as an output for Monochrome displays or printers. In this mode coloured backgrounds are suppressed for viewing clarity. The output is at a low level to display a character.

12. **Character Rounding**

Characters are normally rounded by adding half dots to smooth diagonals. For normal height characters the extra TV lines made available by interlace are utilised for this and so if in non-interlace mode single height characters cannot be rounded.

Character rounding can be inhibited totally by a signal from Control and in this mode, intended specifically for printers, flashing is also suppressed. Reset by P key or new Viewdata page.

13. **Cursor**

The cursor is stored as the 8th bit of the appropriate character in the Data Store. When switched on it is displayed as a bar on the bottom line of the character rectangle flashing between foreground colour and black in anti-phase to normal flashing characters.

14. Non Interlaced Operation

When interlaced composite sync. is input to the chip it operates in normal Interlaced Mode and regenerates Interlaced composite sync.

If there is no incoming sync. the chip switches to the OFF hours mode.

If the Phase Comparator output is pulled high, e.g. 4k7 to Vcc, Interlaced Sync. is output. If the Phase Comparator output is held low Non Interlaced Sync. is output and character rounding for single height characters is inhibited.

SIGNAL DETECTION CRITERIA (For On Hours Operation)

The Video Generator detection circuitry for incoming sync. signals is designed to prevent mis-operation in the presence of noise. The criteria for detection is defined below.

1. Line Sync

The Comp. Video Input must be negative for greater than 3μs.

2. Frame Sync.

The Comp. Video Input must be negative for greater than 12μs and at least 310 lines (Line Flyback pulses) must have occurred since the previous Frame Sync detection.

3. Odd Frame Detection

Odd Frame Detection occurs when a Line Flyback pulse falls in a window 12–39μs after Frame Sync Detection. This is used to lock the line counter.

4. On-Hours/Off-Hours Detection

The incoming line flyback and line sync pulses are compared to determine whether a valid transmission is being received. Lack of coincidences/frame are accumulated and if more than 16/Frame occur for a period 350–1000ms the logic deems that a valid transmission is not being received and the chip switches 'OFF Hours''. If however, less than eight occur in any two successive ½ frames, the logic deems that a valid Composite Sync is being received and the system goes 'ON Hours'.

For the chip to be able to look for synchronism the following phase relationship between Line Flyback and Comp. Sync must be satisfied.

(a) Earliest back edge of LFB is 2μs after leading edge of line sync.

(b) Latest leading edge of LFB is 2μs after leading edge of line sync.

(c) Latest back edge of LFB is 12μs after leading edge of line sync.

The minimum length of the LFB pulse is 8μs.

5. 6MHz Display Oscillator

The 6MHz display oscillator must run fast in the OFF Hours mode but not so fast that the ON/OFF Hours detection criteria cannot be satisfied. This sets a maximum offset of +1.5kHz, the minimum offset is set by lock time criteria and would typically be +0.5kHz.

The frequency range of the oscillator must extend below the 6.0MHz nominal frequency. The minimum frequency should be at least −0.5kHz but can be as low as convenient.

COMPOSITE SYNC INPUT

On chip D.C. restore is provided which allows simple interfacing to the television, either composite sync. signals or video being acceptable.

As the Composite Sync/Video signal from the television may not be referenced to the system earth it is a.c. coupled to the chip.

A typical Interface Circuit is shown in Fig.3.

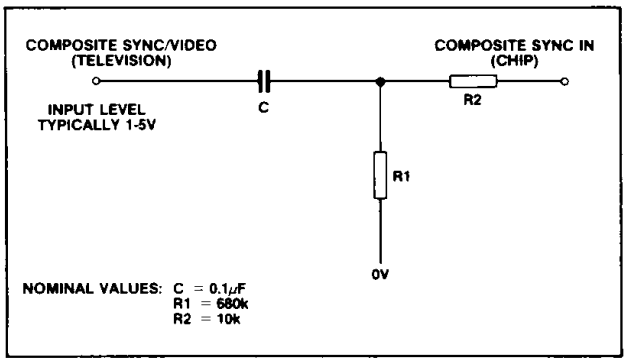


Fig.3 Typical interface circuit

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to Vss . . . . . –0.3 to +15V
Storage temperature range. . . . . –55°C to +150°C

*Exceeding these ratings could cause permanent damage
Functional operation is not guaranteed under these conditions
Operating ranges are specified below

Standard Conditions (unless otherwise indicated)

Vss = 0V (Substrate voltage)
Vcc = +5V ± 5%
Vdd = +10V ± 10%
Operating Temperature (Ta) = 0°C to +70°C
Clock Frequency 6.0MHz

Characteristic	Min	Typ**	Max	Units	Conditions
INPUTS					
Chip Select					
Input Logic High	2.4		Vcc	V	
Input Logic Low	Vss		0.8	V	
Input Current	10	25	100	μA	Vin = 5V
Comp. Sync.					
Input Logic High	1.0		Vcc	V	
Input Logic Low	–0.3		0.05	V	See Note 1
Input Capacitance			15	pF	Vin = 0V
Source Current		50		μA	Vin = 0V
6MHz					
Input Logic High	2.8		Vdd	V	
Input Logic Low	Vss		0.4	V	
Input Capacitance			25	pF	Vin = 0V
Mark to Space Ratio	40:60		60:40		
Frequency	1.0		6.5	MHz	
Input Leakage			10	μA	Vin = 10V
All Other Inputs					
Input Logic High	2.4		Vdd	V	
Input Logic Low	Vss		0.8	V	
Input Capacitance			15	pF	Vin = 0V
Input Leakage			10	μA	Vin = 10V
OUTPUTS					
Addresses, Read/Write					
Store Select (Tri-State) (Note 2)					
Logic High Output	2.4		Vcc	V	Ioh = -300μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 3.0mA
Capacitance			15	pF	Vin = 0V
T rise T fall			200	ns	C load = 200pF
Leakage (Disabled)			10	μA	Vo = 0V, 5V
Time Slots (TS1, TS2)					
(Push-Pull)					
Logic High Output	2.4		Vcc	V	Ioh = -300μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 3.0mA
T rise T fall			200	ns	C load = 200pF
Comp. Sync (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 1.6mA
Logic High Leakage			10	μA	Vo = 10V
Capacitance			20	pF	V0 = 0V
Delay from Comp. Sync In.			1	μs	ON Hours only

Characteristic	Min	Typ**	Max	Units	Conditions
$\overline{\text{RSYNC}}$ (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 4.0mA
Logic High Leakage			10	μA	Vo = 5V
Capacitance			15	pF	Vo = 0V
Phase Comparator (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 4.0 mA
Logic High Leakage			10	μA	Vo = 10V
Capacitance			15	pF	Vo = 0V
R.G.B. Outputs Picture/Text Output (Tristate) (Note 2)					
Logic High Output	Vcc−1		Vcc	V	I source = 1mA
Logic Low Output	Vss		1	V	I sink. = 2mA
Capacitance			20	pF	Vin = 0V
T rise T fall (10%–90%)			30	ns	CL = 30pF
Differential T rise T fall			30	ns	CL = 30pF Note 3
19.2kHz, 1.2kHz Outputs					
Logic High Output	2.4		Vcc	V	Ioh = -30μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 300μA
T rise T fall			1	μs	C load = 100pF
POWER					
Vcc Supply		25	40	mA	Vcc = 5V
Vdd Supply		40	66	mA	Vdd = 10V

Note 1: Voltages below −0.3 volts should be current limited to 1mA.

Note 2: All tristated when $\overline{\text{Chip Select}}$ = Vcc. R.G.B. outputs also tristated when displaying picture and not mixed.

Note 3: Picture/$\overline{\text{Text}}$ matched in mix mode only.

** Typical values are at +25°C and nominal voltages.

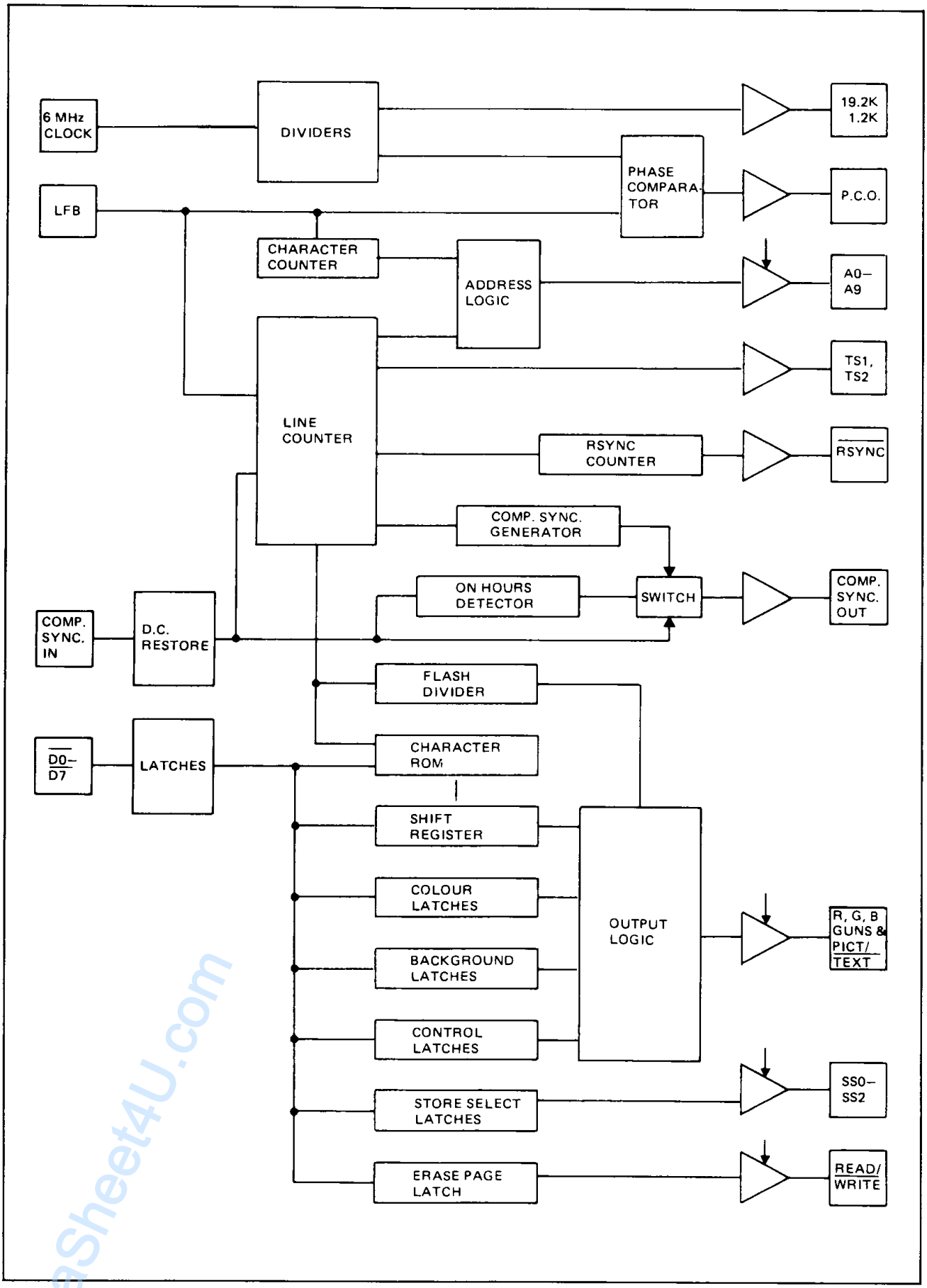


Fig.4 Block diagram

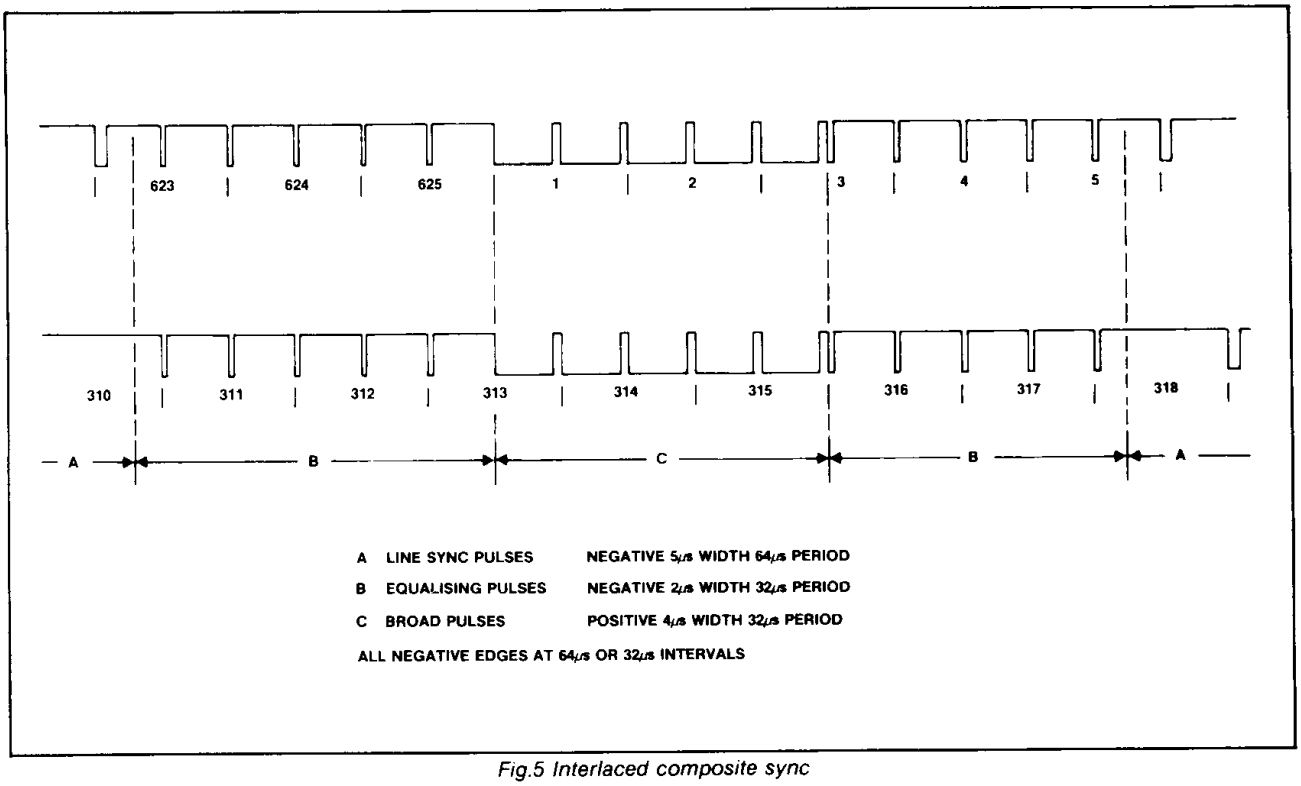


Fig.5 Interlaced composite sync

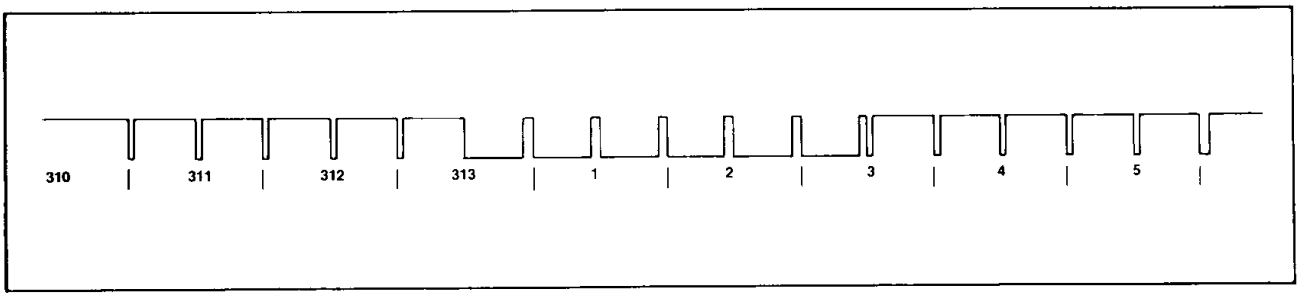


Fig.6 Non interlaced composite sync output

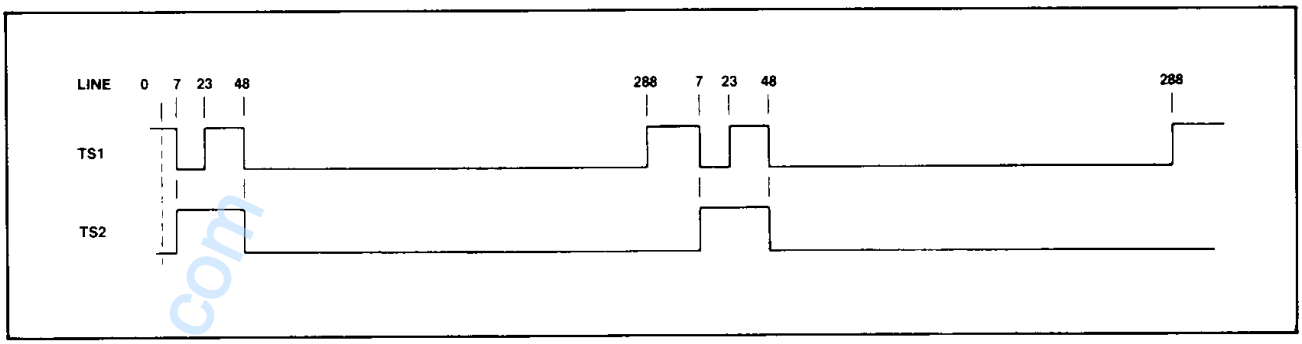


Fig.7 Time slot outputs non interlaced

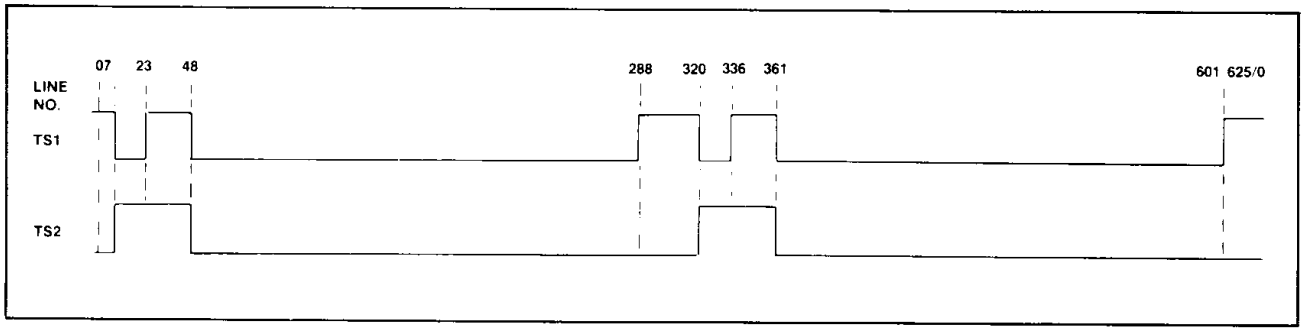


Fig.8 Time slot outputs (interlaced)

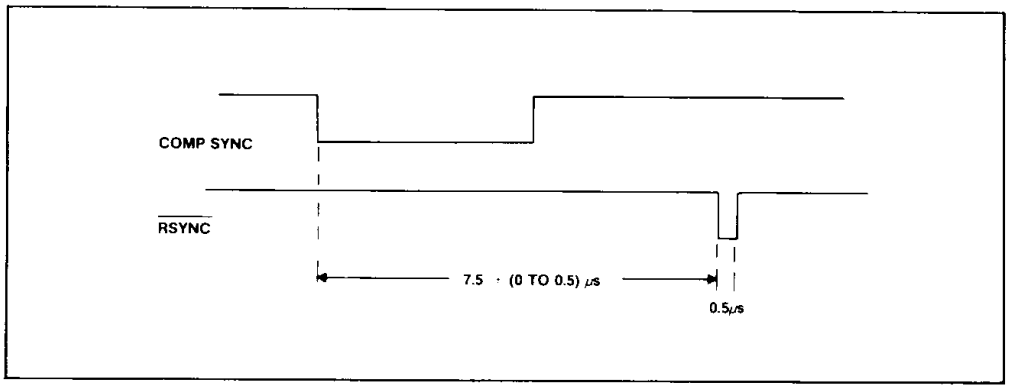


Fig.9 RSYNC timing

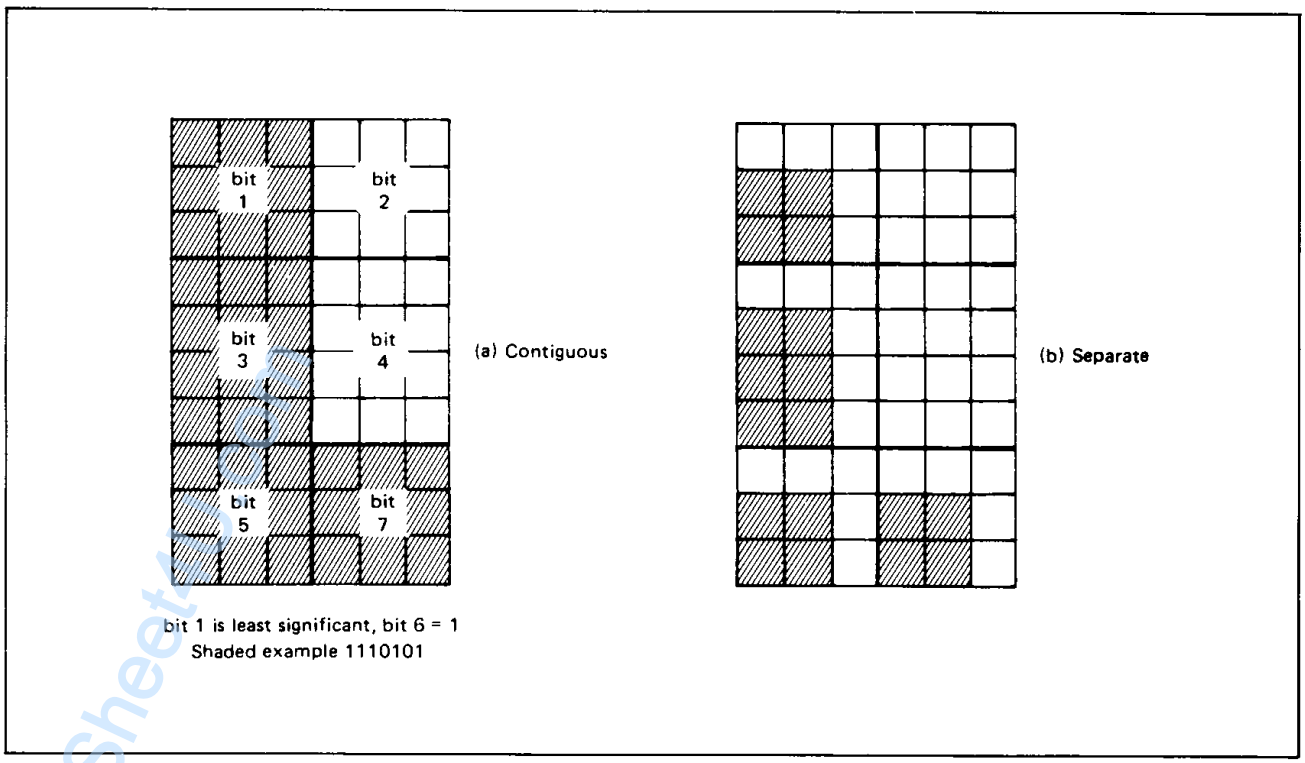
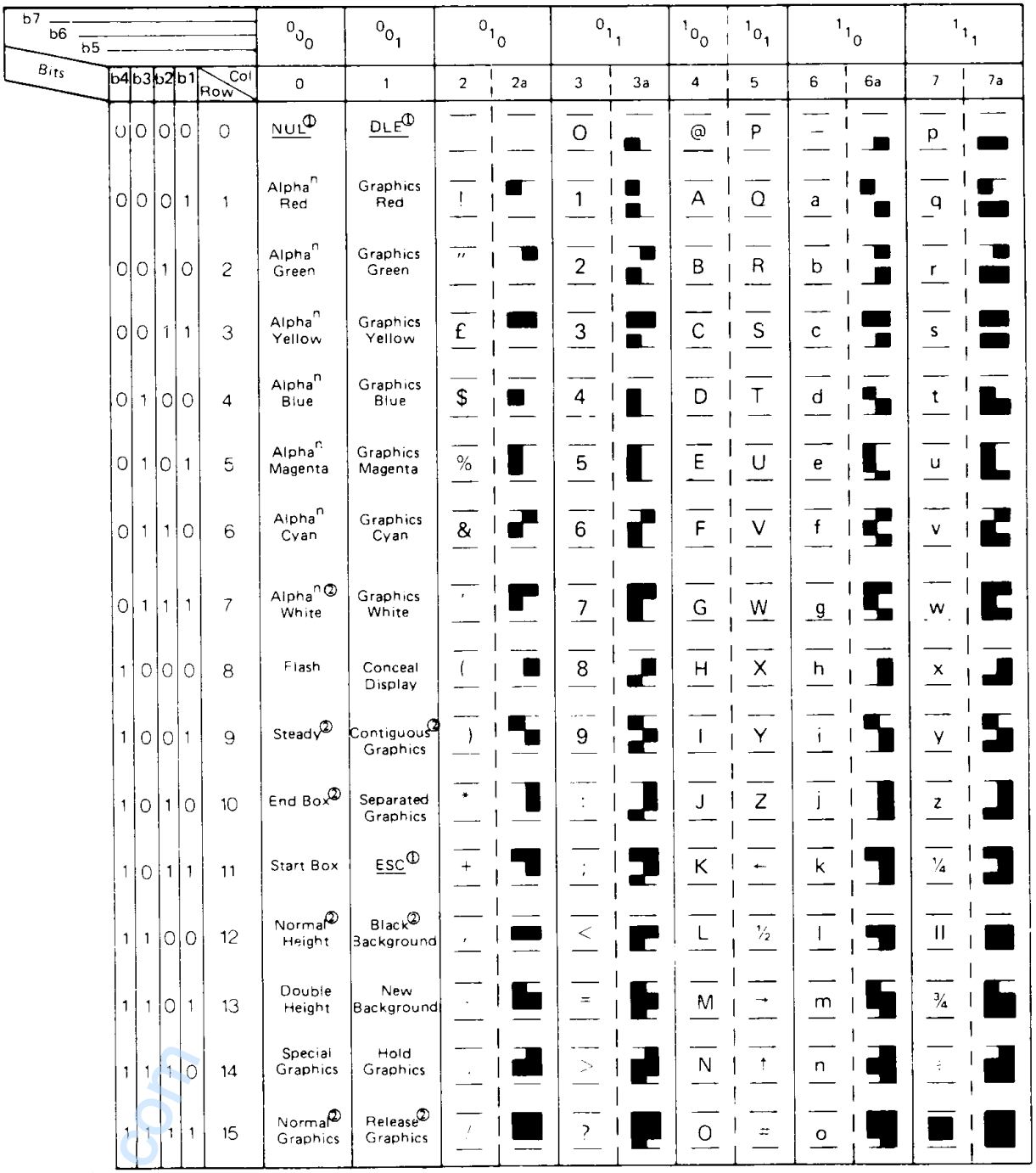


Fig.10 Graphics format



b7 b6 b5 / Bits b4 b3 b2 b1 / Col / Row	0_{0_0}	0_{0_1}	0_{1_0}		0_{1_1}		1_{0_0}	1_{0_1}	1_{1_0}		1_{1_1}	
	0	1	2	2a	3	3a	4	5	6	6a	7	7a
0 0 0 0 / 0	NUL①	DLE①			O		@	P	–		p	
0 0 0 1 / 1	Alpha^{n} Red	Graphics Red	!		1		A	Q	a		q	
0 0 1 0 / 2	Alpha^{n} Green	Graphics Green	"		2		B	R	b		r	
0 0 1 1 / 3	Alpha^{n} Yellow	Graphics Yellow	£		3		C	S	c		s	
0 1 0 0 / 4	Alpha^{n} Blue	Graphics Blue	$		4		D	T	d		t	
0 1 0 1 / 5	Alpha^{n} Magenta	Graphics Magenta	%		5		E	U	e		u	
0 1 1 0 / 6	Alpha^{n} Cyan	Graphics Cyan	&		6		F	V	f		v	
0 1 1 1 / 7	Alpha^{n}② White	Graphics White	'		7		G	W	g		w	
1 0 0 0 / 8	Flash	Conceal Display	(		8		H	X	h		x	
1 0 0 1 / 9	Steady②	Contiguous② Graphics	)		9		I	Y	i		y	
1 0 1 0 / 10	End Box②	Separated Graphics	*		:		J	Z	j		z	
1 0 1 1 / 11	Start Box	ESC①	+		;		K	←	k		¼	
1 1 0 0 / 12	Normal② Height	Black② Background	,		<		L	½	l		‖	
1 1 0 1 / 13	Double Height	New Background	-		=		M	→	m		¾	
1 1 1 0 / 14	Special Graphics	Hold Graphics	.		>		N	↑	n		÷	
1 1 1 1 / 15	Normal② Graphics	Release② Graphics	/		?		O	#	o		■	

① These control characters are reserved for compatibility with other data codes

② These control characters are presumed before each row begins

Codes may be referred to by their column and row e.g. 2 5 refers to %

Character rectangle

Black represents display colour

White represents background

Fig.11 Teletext character codes (002 character set)